SSC8034GSB

N-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
30V	±12V	18mR@10V	7A
		20mR@4V5	
		30mR@2V5	

➢ Description

The SSC8034GSB is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent RDSON with low gate charge. This device is suitable for use in DC-DC conversion and power switch applications.

➢ Applications

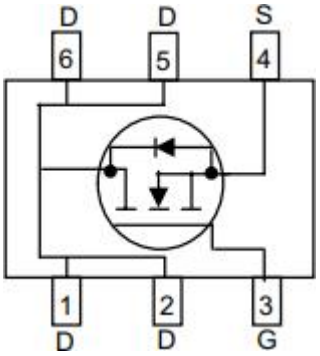
- Load Switch
- Portable Switch
- DCDC conversion
- Charging
- Driver for Relay, Motor, Solenoid, LED etc.

➢ Ordering Information

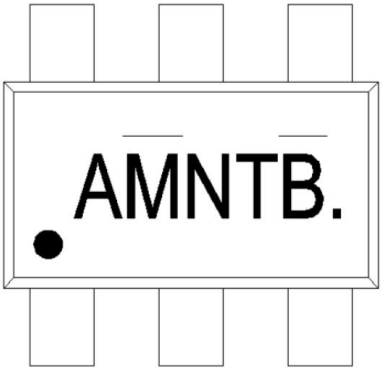
Device	Package	Shipping
SSC8034GSB	SOT23-6	3000/Reel

➢ Pin configuration

Top view



Bottom View



Marking

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	30	V
V_{GSS}	Gate-to-Source Voltage	±12	V
I_D	Continuous Drain Current [a]	7	A
I_{DM}	Pulsed Drain Current [b]	28	A
P_D	Power Dissipation [c]	1.7	W
P_{DSM}	Power Dissipation [a]	0.9	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		155	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		80	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

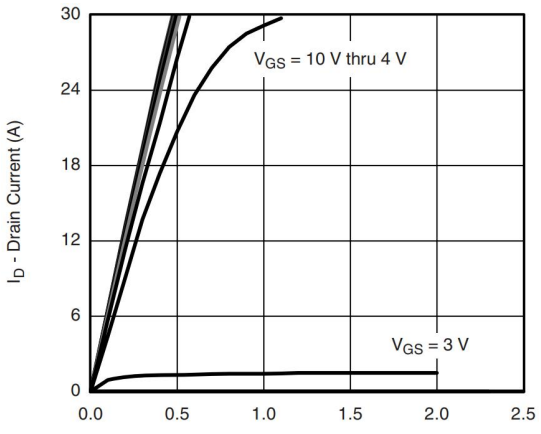
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

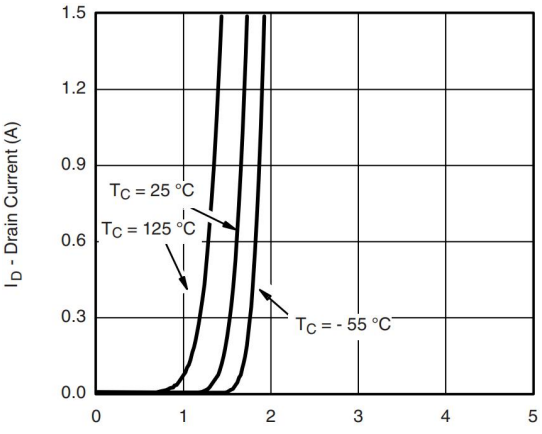
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=250uA	30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=250uA	0.7	1	1.4	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=10V,ID=5A		18	30	mR
		VGS=4.5V,ID=4A		20	35	
		VGS=2.5V,ID=3A		30	55	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=24V,VGS=0V			1	uA
I_{GSS}	Gate-Source leak current	VGS=±12V,VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=5V,ID=3A		10		S
V_{SD}	Forward Voltage	VGS=0V,IS=1A		0.7	1.4	V
Ciss	Input Capacitance	VDS=15V, VGS=0V, f=1MHz		700		pF
Coss	Output Capacitance			300		
Crss	Reverse Transfer Capacitance			260		
$T_{D(ON)}$	Turn-on delay time	VGS=10V, VDS=15V,ID=3A		19		ns
Tr	Rise Time			9		
$T_{D(OFF)}$	Turn-off delay time			65		
Tf	Fall Time			20		
Qg	Total Gate charge	VGS=10V, VDS=10V, ID=3A		10.6		nC
Qgs	Gate Source charge			1.9		
Qgd	Gate Drain charge			2.1		

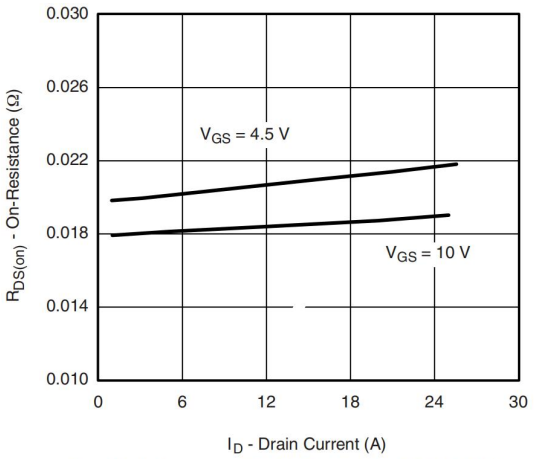
➢ Typical Characteristics(T_A=25℃ unless otherwise noted)



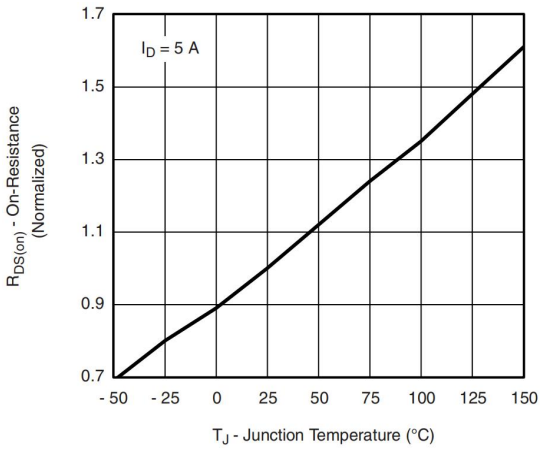
Output Characteristics



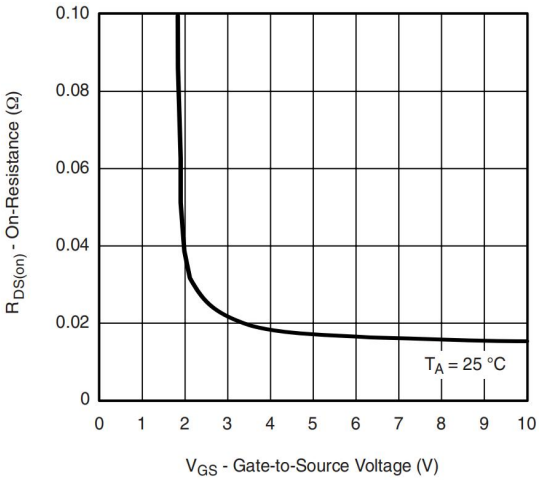
Transfer Characteristics



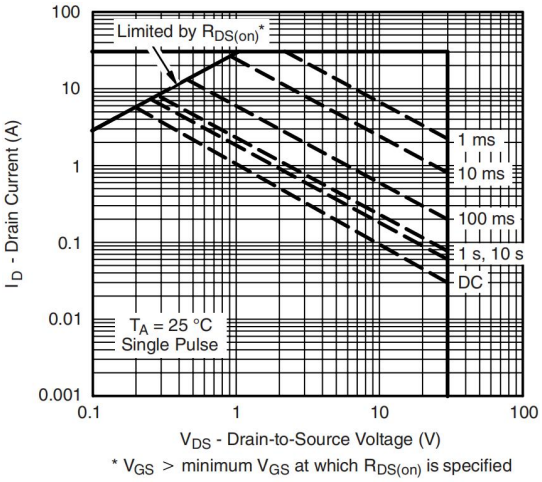
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Junction Temperature



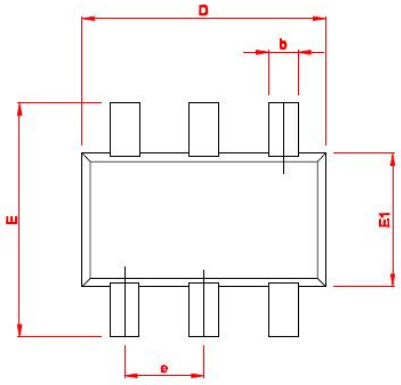
On-Resistance vs. Gate-to-Source Temperature

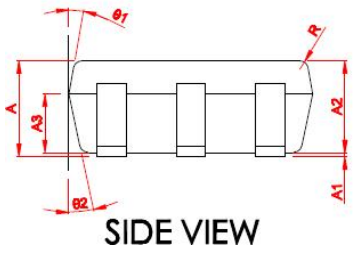


* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

➢ Package Information





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.15	1.24
* A1	0.01	0.05	0.09
* A2	1.05	1.10	1.15
A3	0.65	0.70	0.75
* b	0.30	0.35	0.45
* c	0.117	0.127	0.157
* D	2.87	2.92	2.97
* E	2.72	2.80	2.88
* E1	1.55	1.60	1.65
* e	0.90	0.95	1.00
* L	0.32	0.40	0.48
* L1	0.55	0.60	0.65
R	0.10 REF		
R1	0.12 REF		
* θ	0	--	8°
θ1	8°	10°	12°
θ2	10°	12°	14°

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